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RESEARCH OF THE SIGMA-T ANALOG-TO-DIGITAL CONVERTER WITH COMBINED COMPENSATING OF THE ERROR FROM EDGE EFFECTS

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Abstract

Relevance and goals. Information converters with sigma–Δ architecture have nowadays the biggest conversion function linearity. However, absence of opportunity of accurate measures results aligning to their time caused by necessity of one bit sequence on sigma–Δ modulator outcome digital filtration, reduces possibilities of their use in measure tasks. This work’s goal is to realize the algorithm of information conversion to ADC of sigma-architecture where the intermediate pulse-width modulated signal is summoned in ranging conversion cycles in time that exceeds periods of impulse modulation greatly. That is done to exclude modulator outcome signal digital filtration. Such information converters are called sigma-T ADC.

The researches are made on computer model level where we use combined (analog-to-digital) way of errors caused by edge effects compensation. It gives us an opportunity to summon up intermediate conversion cycles results without accumulating errors that let us to give up filtration procedure.

Materials and methods. In this article we study a combined way of errors caused by edge effects compensation in integrating sigma-T ADC. A computer model was made in Simulink...
environment. We defined standard deviation from conversion linear function, both with and without compensation of errors caused by edge effects.

**Results.** The opportunity is shown for realization of sigma-T ADC with conversion high precision for solving tasks of data-measuring equipment. Here we give calculations results of standard deviation from conversion linear function for integrating sigma-T ADC both with and without errors compensation.

**Conclusion.** The worked out model of integrating sigma-T ADC showed possibility of good metrological characteristics of measuring converter without using digital filtration of the outcome signal.

**Keywords:** integrating sigma-T ADC, error compensation, computer model, edge effect, conversion function linearity, sigma-∆ modulation, standard deviation.

**Introduction**

When realizing multibit precision ADC they use nowadays methods of intermediate compensating integrating voltage conversion to a signal of one of impulse modulation kinds: pulse-width (PWM), pulse-frequency (PFM), pulse-position (PPM), pulse-code (PCM), differential pulse-code (DPCM) signal [1, 2]. The latter kind of intermediate modulation is well known as sigma-delta modulation due to advantages of the technology and digital signal processing methods [3-5]. To get the conversion results of information converters with sigma-architecture, intermediate modulated impulse signal is summoned up for a few ranging conversion cycles which length exceeds impulse modulation greatly [2-4]. When the conversion time (summoned results of intermediate conversion) is increased, potentially higher resolution and linearity of conversion function can be reached. However, there are some serious restrictions concerning a number of methodical errors including edge effects errors [6, 7]. Besides, when realizing information conversion into ADC with sigma-delta architecture a problem appears concerning measures results aligning to the conversion time that reduces possibility of their use for solving measuring tasks [8].

**Realization of combined method of edge effect error compensation**

Some new ways of integrating analog-to-digital conversion [9, 10] were offered for reducing conversion methodical errors caused by edge effects that would exclude edge effects errors and improve metrological characteristics of integrating ADC.
Offered structural algorithmic method presupposes, as well as traditional one, summation of intermediate signals during conversion period. To correct errors in a short period of time ranging to the end of conversion period, the integrator is penetrated with degenerative feedback through operational amplifier and an amendment is added, proportional to the outcome impulse at operational amplifier [9].

The method realization is illustrated with functional scheme and time diagrams of integrating ADC work given in pic. 1 where WFGо is weight function generator for voltage reference \( g_о(t) \), \( M_о \) – multiplier of reference voltage \( U_o \) to weight function \( g_о(t) \), \( M_u \) – multiplier of transformable voltage \( u_x \) to weight function \( g_x(t) \), WFGх – weight function generator for transformable voltage \( g_x(t) \), WFGс – weight function generator for correcting voltage, Sw for switch, three adders, I – integrator, CT – comparison tool, TLG – threshold level generator, CP – control panel, DI – digital integrator (impulse counter), RFG– reference frequency generator, additional integrator \( I_A \) and additional comparison tool CT\(_A\).

In pic. 1, \( b \) and \( c \) a piece of time diagram is given showing processes which take place in the ADC at the end of each full conversion cycle.

Bald vertical line marks the border between two neighbor full conversion cycles. In the diagram \( I(t) \) is an output signal of the main integrator I, \( u_f(t) \) – a signal formed in the outcome of FLG and setting threshold level for CT.

ADC conversion equation can be shown like below:

\[
\frac{1}{T_c} \int_{t_b}^{t_e} g_x(t)u_x(t) dt + \frac{1}{T_c} \int_{t_b}^{t_e} g_о(t)U_о dt = I(t_e) - I(t_b),
\]

\[
\frac{1}{RC} \int_{t_b}^{t_e} g_x(t)u_x dt - \frac{1}{RC} \int_{t_b}^{t_e} g_о(t)U_о dt = \Delta I,
\]

where \( RC \) is a constant of time integrator I that sets the scale of signals integration \( g_xu_x \) and \( g_оU_о \); \( u_x \) and \( U_o \) – transformable and reference voltage accordingly; \( T_c \) – the length of the full conversion cycle; \( g_x \) – weight function of transformable voltage (in the simplest case while realizing rectangular weight function \( g_x = 1 \)); \( g_о \) – weight function of reference voltage; \( \Delta I = I(t_e) - I(t_b) \) – residual of values in the main integrator outcome in the the beginning and the end of each full conversion cycle. Weight function coincides \( u_f(t) \) signal, and its module equals 1.
Picture 1. Functional diagram of ADC with edge effects errors compensation (a) and appropriate time diagrams (b, c).
Let's make $U_x$ the average value of incoming voltage in the full cycle. Then we will get the following as the result of integrating ADC conversion from equation (1):

$$\int_{t_1}^t g_x(t)dt = \frac{U_T}{U_o} \frac{RC}{U_o} \Delta I.$$  

Let's suppose that in the beginning of the full cycle the voltage in the main integrator outcome equals $U_T$ ($U_T$ – amplitude of threshold signal $u_T(t)$). Then according to time diagram in pic.1 b $\Delta I = I(t_c) - I(t_b)$ value equals $U_T - I(t_b)$ residual. Equation (2) implies that if $\Delta I \neq 0$ the result of ADC conversion contains additive error that is called edge effects error. For its correction you need to subtract value of amendment $(RC/U_0)\Delta I$ from conversion result (2). It is done in the following way. In the period between the end of the full conversion cycle and the moment of main integrator outcome voltage reaching positive threshold level a signal is given to the additional integrator $I$, the same as to the main integrator income. After that the multiplication $g_c U_o$ goes to the main integrator income where $g_c$ is correcting weight function (constant index). Let's find conversion equation that is made with additional conversion channel including blocks $WFG_c$, $I_A$ and $CT_A$:

$$\int \int \frac{1}{R_a C_a} \int g_o(t)U_o dt - \frac{1}{R_{aC_a}} \int g_x(t)U_o dt - \frac{1}{R_{aC_a}} \int g_o U_o = 0.$$  

where $R_a C_a$ is a time constant of the additional integrator.

As far as we have $g_x = 0$ and $g_o(t) = 0$ on the interval $[t_c, t_1]$ (switch Sw is open only in the interval $[t_c, t_1]$), then the equation (3) can be written in the following way:

$$\int \int \frac{1}{R_a C_a} \int g_o(t)U_o dt - \frac{1}{R_{aC_a}} \int g_x(t)U_o dt - \frac{1}{R_{aC_a}} \int g_o U_o = 0.$$  

If count the correlation $R_{aC_a} = RC$ than it is obvious that first two addends show main integrator outcome voltage increase in interval $[t_c, t_1]$, i.e. value $\Delta I = I(t_c) - I(t_b)$. Now let's count the equation (4) concerning value of informative interval $\Delta T = t_2 - t_1$

$$\Delta T \frac{R_{aC_a}}{g_o U_o} \Delta I.$$  

The first part of the equation (5) contains $\Delta I$ that let us use $\Delta T$ value as an amendment added to the result (2) to exclude edge effects error. With the amendment the equation looks like below:

$$\int \int \frac{1}{R_{aC_a}} \int g_o(t)U_o dt - \frac{1}{R_{aC_a}} \int g_x(t)U_o dt - \frac{1}{R_{aC_a}} \int g_o U_o = 0.$$  

The equation (6) shows that there will be no edge effects error if:
It's obvious from the equation (7) that $ WF_g \leq 0 $ that suits amendment entry algorithm logic.

Let's suppose that the end of the cycle following the considered one comes at the moment when the main integrator outcome voltage reaches $ +U_T $ value. It is quite obvious that in this case in the conversion equation (1) $ \Delta I $ value equals residual $ I(t_e) - I(t_b) $ in the previous cycle. That means that for excluding of error caused by inequality of the main integrator outcome voltage to $ +U_T $ value in the beginning of the full cycle you can add the amendment due to the equation (6) where $ \Delta I $ value equals residual $ I(t_e) - I(t_b) $ in the previous cycle. One of the variants to enter this amendment is multiplication $ g_c U_o $ getting through the second adder to the main integrator income in interval $ \Delta T $. Then conversion equation can be written like:

$$ \int \int g_c U_o dt - \int \int g_c(t) U_o dt + \frac{g_c U_o \Delta T}{RC} = \Delta I. $$

(8)

It follows from equation (5) that:

$$ g_c U_o \Delta T = R_a C_a \Delta I. $$

(9)

Let's add $ g_c U_o \Delta T $ value to equation (8) according to equation (9), we will get:

$$ \int \int g_c U_o dt - \int \int g_c(t) U_o dt + \frac{R_a C_a \Delta I}{RC} = \Delta I. $$

(10)

That means that there will be no edge effects error if

$$ R_a C_a = RC. $$

(11)

Model of this method is illustrated in pic.2.
The model realizes two full conversion cycles with separate formation of two results. Cycle(B) subsystem is used to form two consequent intervals determining full cycle length. Its diagram is given in pic. 3.

Integrator1 has presetting of minus outcome value. That gives opportunity to move the full cycles regarding the beginning of the model time by changing this parameter. The end of the
movement time fits the moment of Relay2 block switch. That
happens at the moment of the integrator outcome value passing zero
position.

Constant outcome value goes to the minus income of the
first (left) adder. As a result Relay3 block switches when the
integrator outcome value equals Constant outcome value. This
moment coincides the end of the first full conversion cycle.
Constant block outcome value multiplied by 2 with help of Product
block goes to the second adder minus entry. As a result Relay1
switches at the moment of the end of the second full conversion
cycle. Blocks NOT and AND form two impulses that length is equal
to the full conversion cycle, and the first impulse trailing edge
coincides the second impulse leading edge (i.e. appropriate periods
are ranging). The first impulse is formed in Out1 of Cycle(B)
subsystem, while the second one in Out2.

ControlBlock2 subsystem is similar to ControlBlock1
subsystem. They both are aimed to form supporting signal as a
positive single differential that front coincides the end of appropriate
full conversion cycle (on time diagrams this signal is marked with
the letter D).

ConvertTime1 subsystem has the same goal as
ConvertTime – getting the full conversion cycle length in the same
units as informative periods are measured.

The amendment value is found with help of Corr1
subsystem due to time diagrams in pic. 1, b and c. The subsystem
diagram is given in pic.4.

![Corr1 subsystem diagram](pic.4)

Time interval $t_e - t_f$ (pic. 1, b and c) is formed with help of
tend_t1 subsystem, which is a part of Corr1 subsystem. Tend_t1
subsystem diagram is given in pic.5.
Signal D from ControlBlock1 subsystem outcome goes to income In1, while Relay block impulse goes to In3 (pic.2), that leading edge coincides the moment of the Integrator outcome value reaching $+U_T$ value (on the model in pic. 2 its value is given by Treshold1 block). These signals go to the AND circuit (LO1 in pic. 5). AND circuit outcome impulse sets R5-trigger S-R1 (pic. 5) to zero position (its original position is 0) with its leading edge. Q-trigger S-R1 outcome signal and D signal go to the AND circuit income (LO4 in pic.5), as a result an impulse with length $t_{1-t_e}$ (pic.1, b and c) is formed in its outcome. Transport delay block TD, NOT circuit (LO2 in pic.5) and AND circuit (LO3 in pic.5) form a short impulse that leading edge coincides the trailing edge of the impulse with length $t_{1-t_e}$. All described above is illustrated by oscillogram in pic. 6, which was gotten with help of oscilloscope Scope in pic. 5.

The rest of Corr1 subsystem realizes conversion due to the second lines of time diagrams in pic. 1, b and c forming as a result informative impulse with length $\Delta T$. During the interval $t_{1-t_e}$ (pic.1, b and c) Out1 outcome signal of tend_t1 subsystem goes to Switch1 control income what results in a signal going to the additional integrator through scaling block Gain which is the same as the signal going to the main Integrator income (pic.2). When the interval $t_{1-t_e}$ is over S-R1 trigger is switched to $Q=1$ condition by a short impulse from Out2 outcome of the tend_t1 subsystem (pic.3). When the outcome value of this integrator reaches zero level (moment $t_2$ in pic.1, b and c), Relay block switches from 0 position to position 1. It's important that additional integrator outcome value was shifted slightly (it is 0.0000001) in order to keep relay block in zero position up to the chosen moment. NOT circuit, transport delay block and AND circuit (LO1, TD and LO2 in pic.3) form a short impulse that leading edge coincides the moment of Relay block switch. This
impulse returns S-R1 trigger to the zero position finishing the informative interval $\Delta T$.

![Scope block oscillograms.](image)

Corr2 subsystem diagram is similar to Corr1. So, as it was described above, two intervals are formed in the model which define two full conversion cycles. First cycle result is fixed on display DisplResult1 (pic.2). During the first full cycle informative intervals go from S-R trigger through AND circuit (L4 in pic.2) and further through scale block Gain2 to Integrator2. In CalcResult1 subsystem we get an equivalent of transformable voltage as a proportional value

$$\sum (T_{j} - T_{i}) = T_{c} - 2 \sum T_{i},$$

where the summation takes place in interval $T_{c}$.

CalcResult1 subsystem outcome result contains edge effects error and is fixed by block DisplResult1. Block DisplT1iSum is necessary for the model adjusting and it fixes value proportional to $\sum T_{i}$.

Similar result is gotten during the second full cycle with blocks L6, Gain4, Integrator1 and CalcResult2 (pic.2). The amendment in the form of intervals $\Delta T$ formed by blocks Corr1 and Corr2 are scaled to the main results with blocks Gain5, Integrator3 and Gain4, Integrator1. The first amendment is summoned with the
main result with «+», the second one with «-». The result with the amendments is fixed by block DisplResult5.

**Conclusion**

After processing the experiment results the following standard deviation values for ADC (relatively low significant bit), both with and without edge effects error compensation (Table 1).

<table>
<thead>
<tr>
<th>Number of steps of modulation in a full cycle</th>
<th>Standard deviation for ADC without edge effects error compensation</th>
<th>Standard deviation for ADC with edge effects error compensation</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.5398</td>
<td>0.0317</td>
</tr>
<tr>
<td>100</td>
<td>0.0980</td>
<td>0.0067</td>
</tr>
<tr>
<td>1000</td>
<td>0.0138</td>
<td>0.0003</td>
</tr>
</tbody>
</table>

Thus, the examined structural algorithmic method of edge effects error compensation truly reduces standard deviation of quantization distortion and increases conversion linearity.

**References:**

4th the International Conference on the Transformation of Education 2016


